AMENDMENT

In the Specification:

Kindly replace the paragraph on page 2, starting on line 13 with the following paragraph, wherein the word insulator is added for clarification, without prejudice.

BRIEF SUMMARY OF THE INVENTION

Accordingly, the present invention provides a dual gate semiconductor device, such as a FLASH memory semiconductor device, whose plurality of dual gate sidewall spacer structure are not formed from traditional dielectric material similar to the anti-reflective coating material that is traditionally used for lithographic patterning. Rather, the present invention provides a dual gate semiconductor structure whose sidewall spacers are formed by a first and second anti-reflection fabrication process, whereby, the sidewall spacers of the dual transistor gate structure in the core memory region are left coated with the second anti-reflective coating material, such as silicon oxynitride (SiON), silicon nitride (Si_3N_4), and insulator silicon germanium (SiGe), or other material having optical properties compatible with subsequent fabrication processing, to form sidewall spacers for use in subsequent implant and salicidation steps, commonly used during fabrication of the semiconductor device being formed. Other features of the present invention are disclosed or are apparent in the section entitled "DETAILED DESCRIPTION OF THE INVENTION."

Kindly replace the paragraph on page 4, starting on line 16 with the following paragraph, wherein the word insulator is added for clarification, without prejudice.

Figure 4 shows the present invention, where, in preparation for subsequent patterning processes, a second coating of anti-reflective coating material 17, such as silicon oxynitride (SiON), silicon nitride (Si_3N_4), and insulator silicon germanium (SiGe), or other suitable material with dual purpose optical properties compatible with other fabrication processes, is deposited in a thickness in a range of 300Å to 1000Å over the core memory stacks 12 and 13, the spacing S between stack 12 and 13, floor region F, the core-periphery interface region CP, and over the periphery memory region 9. As shown in Figure 5, the second coating 17 is used for patterning any remaining gate structures, such periphery gate structures 7 and 8

Cmd D2

in the periphery memory region 9, depicted in Figure 4, by appropriate masking and etching operations.

Kindly replace the paragraph on page 4, starting on line 26, continuing on page 5 with the following paragraph, wherein the word insulator is added for clarification, without prejudice.

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Figure 6 shows the present invention where spacers 18 are defined on the sidewalls of the core memory gate structure 12 and 13 after stripping the second anti-reflective coating 17 from over the second polysilicon layers P2 of core memory gate stacks 12 and 13, and from over the periphery memory gate structures 7 and 8. Accordingly, the present invention provides a dual gate semiconductor structure 200 whose sidewall spacers 18 of core memory gate structures 12 and 13 are formed by a first and second anti-reflection fabrication process. In accordance with the present invention, the sidewall spacers 18 of the dual transistor gate structure in the core memory region are left coated with the second anti-reflective coating material, such as silicon oxynitride (SiON), silicon nitride (Si_3N_4), and insulator silicon germanium (SiGe), or other material having optical properties compatible with subsequent fabrication processing, to form sidewall spacers for use in subsequent implant and salicidation steps, commonly used during fabrication of the semiconductor device.